Manufacturing an Extremely Efficient Transistor for Decarbonization

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ABSTRACT

"Electrify everything" is a key strategy to decarbonize the economy (when combined with a switch to a net-zero carbon grid) that also is heavily dependent on microelectronics. But growth in microelectronics for sensing, the Internet of Things (IoT) and other edge computing means energy efficiency of microelectronics itself from improvements related to shrinking the size of the transistor may not counter this growth. In the past decade, the most advanced (smallest) conventional transistors have reached the physical limit of low-voltage operation, and thus the path to ubiquitous electrification also risks significant increases in energy consumption. A new transistor technology, the tunnel field effect transistor (TFET), uses ultra-low power quantum tunneling to potentially operate at 1/10th the power of the most advanced conventional transistors. Lower-than-projected energy efficiency due to manufacturing limitations, along with low speed stemming from low current density compared to the established commercial technology (complementary metal oxide semiconductor – CMOS), have prevented the widespread adoption of TFETs. Sandia's innovations, based on work in atomically precise advanced manufacturing (APAM), promise to lower the voltage of the TFET and reach the TFET's promised energy efficiency, while also increasing its current and hence speed. AMO is supporting Sandia to show that an APAM TFET can be manufactured in a way that best leverages existing infrastructure in silicon CMOS processing. Here, we compare TFETs to other candidate energy efficient transistor technologies, and present Sandia's progress towards the APAM TFET. We also discuss future research needs for extreme energy efficiency in microelectronics.

Introduction

Climate impacts caused by exponentially increasing anthropogenic greenhouse gas (GHG) emissions are becoming one of the major challenges we face as a planet. In April 2021, the U.S. Department of Energy's Advanced Manufacturing Office (AMO) added a decarbonization goal to its energy efficiency goals, (DOE/AMO 2021a) as its contribution to Departmental priorities to combat the climate crisis, create clean energy jobs, and promote energy justice (DOE 2021). Specifically, the AMO efficiency and decarbonization goals are 1) Improve the productivity, competitiveness, energy efficiency, and security of U.S. manufacturing; 2) Reduce the life-cycle energy and resource impacts of manufactured goods; and 3) Accelerate emerging and transformative technologies needed to approach net-zero greenhouse gas emissions in the industrial sector by 2050. While the TFET's main contribution initially is to goal 2 because of the increasing pervasiveness of microelectronics in manufactured products, as industry electrifies and becomes "smarter", it will increasingly contribute to the other goals. Manufacturing generates 12 percent of U.S. gross domestic product (BEA 2020) and employs over 12 million Americans (BLS 2021). The U.S. manufacturing sector also has an

annual energy bill of about $200 billion and uses more than one-quarter of primary energy in the U.S. (EPA 2020a, 2020b).

"Extreme energy efficiency technologies" as used it in this paper, are technologies that use at least an order of magnitude (>10x) less energy than traditional technology.Such technologies may be needed to reduce GHG emissions as part of a decarbonization strategy. Analyses have shown that using energy efficiency alone, it may be possible (Nadel and Ungar, 2019; Kaarsberg, Hopson, and Clay, 2004) to halveU.S. GHG emissions[1] (Kerry 2021). But to meet the Biden Administration's goal of reducing our GHG emissions to zero by 2050 (DOE 2021) – another key decarbonization strategy – electrification *with* zero emissions renewable energy, may be necessary (Roberts 2017). Thanks in part to U.S. Department of Energy (DOE)-funded renewable energy technology research, development, demonstration and deployment (RDD&D), reducing electricity-related GHG emissions to zero using renewable power sources has become a key strategy. Electrification in industry, combined with "Smart Manufacturing", may lead to decarbonization while increasing efficiency and performance and lowering cost (CESMII 2021).

Transistors and Circuits, and Chips—Oh My!

As the most basic device, transistors are at the bottom of the "stack" comprising modern microelectronics (Figure 1, below) that support computing and a host of other information and communications technology (ICT) applications—while it's important to improve the energy efficiency of everything in the "stack", improvments in transistor energy efficiency are foundational. A new type of extremely energy efficient transistor combined with improvements in energy efficiency throughout the stack and the entire ICT sector are needed to make microelectronics-powered innovations sustainable. In this paper, we discuss a transistor technology—the Tunnel Field Effect Transistor (TFET)—that could contribute to extreme energy efficiency in microelectronics. As we will show, even though ICT now accounts for only a few percent of energy use, that energy use has been doubling every three years and extreme energy efficiency is needed to flatten and eventually reverse the trend in microelectronics energy use shown in Figure 2. Thus, a TFET contributes to decarbonization through both extreme energy efficiency and better performing smart technologies for electrification.

[1] Specifically on Earth Day 2021, the Biden-Harris Administration declared an aggressive new commitment for fighting climate change: cutting its greenhouse gas emissions by 50 to 52 percent relative to 2005 levels in less than a decade. To do this, the country will have to dramatically increase its energy efficiency and electrify. The analysis doesn't lay out a figure for the outlay but estimates that these changes would add $570 billion per year to the US economy via creating new jobs and avoiding pollution and health problems associated with fossil fuels.

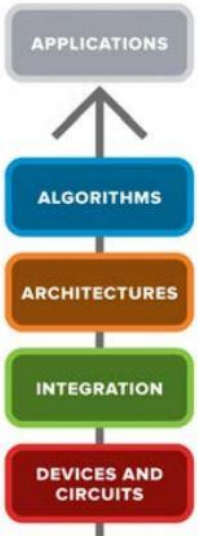

Figure 1: Micro-electronics Stack *Source*: DOE/BES 2021.

Semiconductor-Powered Energy-Efficient Industrial Electrification

"Electrify everything" is a key strategy of decarbonizing industry up and down the supply chain. The industrial sector contributes 22% of greenhouse gas emissions in the U.S. and is a challenging sector to decarbonize through electrification, as many key fossil-fired processes lack a commercial cost-effective electrified alternative (DOE/AMO 2021d). Decades of DOE work on electric vehicles and the batteries and semiconductors to power them has shown how critical semiconductors are to the electrification of a major sector. Just as the dramatic increase in the use of electronics first appeared in hybrid and then electric cars, so too will the use of electronics—primarily for sensors and controls—be greatly expanded as key decarbonizing sectors of industry move to electricity-based processes powered by zero-GHG renewable power.

AMO learned in its first workshop on Semiconductor R&D for Energy Efficiency that improvements in integrated sensor systems, powered by microelectronics, can enhance electrification of industry in three major ways 1) improving electric powered manufacturing processes themselves and making them more energy efficient through sensors and controls; 2) enabling system benefits such as the ability of robust wireless sensors and controls to enable efficient continuous manufacturing even in harsh service environments and 3) direct energy reduction benefits of sensor/control systems that can avoid expensive transmission of data by processing it at "the edge" (DOE/AMO 2021b). Increasing use of the latest semiconductor technologies can lower the cost and increase the performance of electricity-based processes that will need to replace traditionally fossil-fuel-fired industrial processes. Also at the workshop, the head of the Semiconductor Research Corporation (SRC) pointed out that extreme innovation in semiconductors is needed in order to fully realize the potential of ICT including Industry 4.0 (robotics, automation, and advanced manufacturing) and the rise of 5G+. Of course, transistors are not the only source of this innovation, but they are a fundamental building block.

Avoiding Semiconductor Energy Use Explosion via Extreme Energy Efficiency

Semiconductor industry products power nearly every aspect of our lives and will only become more indispensable with the rapid digitization of our modern economy in a post-pandemic world. As we approach the end of Moore's law's efficiency increases and as large industries such as telecommunications, IoT, and manufacturing integrate more advanced semiconductor products into their products and processes, semiconductor energy use is on track to become a major fraction of planetary energy use. As shown in Figure 2, since 2010, computational energy use has doubled nearly every 3 years (SRC/SIA 2021). Ultra-energy efficient semiconductor devices and architectures must be commercialized before 2030 to curb this unsustainable use of energy. Rapid deployment of emerging hardware technologies based on new physical properties is required to prevent electrical energy use from reaching the unsustainable market dynamics limit.

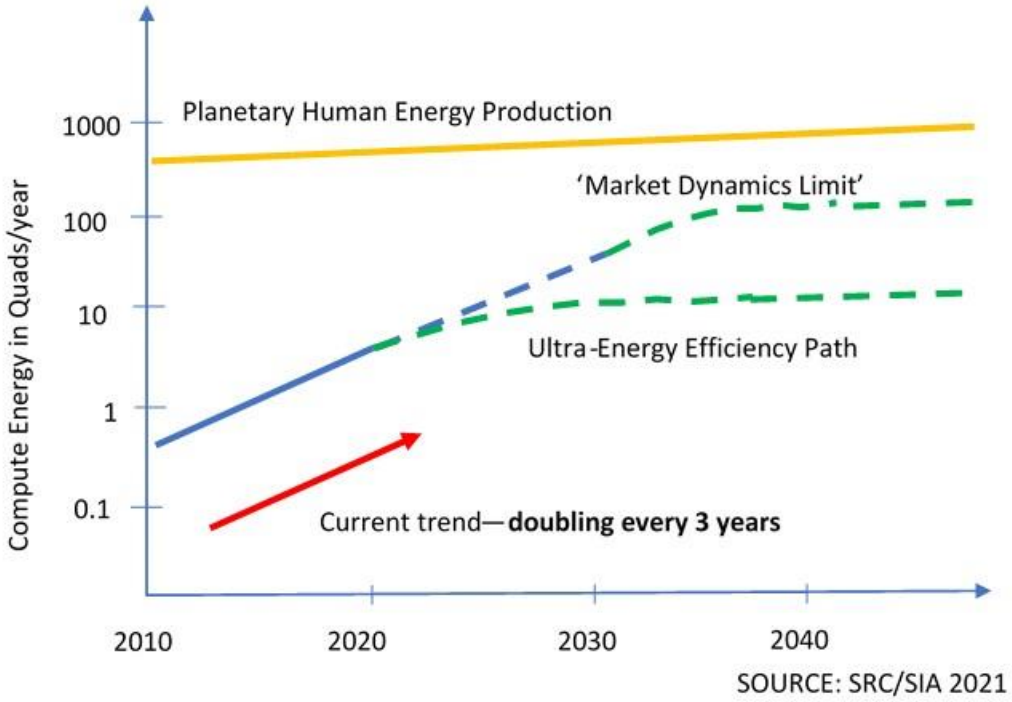

Figure 2: At current growth rates for computational energy use, the Semiconductor Research Corporation (SRC) projects that the "Market Dynamics Limit" will be reached by 2035, limiting the world's computing capacity and economic growth. Alternatively, if extreme-energy efficiency in semiconductor products is prioritized, a trajectory where computing/economic growth and energy use are decoupled can be achieved. *Source*: SRC/SIA 2021.

The looming planetary semiconductor energy impact also comes at a time when the Biden-Harris Administration is accelerating the US response to the climate crisis. RDD&D for semiconductors—including the underlying manufacturing technologies for the next generation of devices—can help avoid a planetary energy problem while accelerating our transition toward sustainable solutions that can revitalize a key domestic industry that offers high-paying jobs. While U.S. firms account for nearly 50 percent of semiconductor sales, only 12% of semiconductor manufacturing occurs in the U.S. (SIA 2020). By demonstrating and deploying

extremely energy efficient transistors, we can combat the climate crisis through reduced energy consumption and electrification across all sectors that use semiconductors by 2030.

Transistors in Microelectronics and Computing

An input voltage on the "gate" of a "solid-state" transistor—made of semiconducting silicon—results in a large current on the "drain" side of the transistor by providing a conducting path for electrons (in an n-type device) or holes (in a p-type device) between source and drain contacts. A transistor is a switch where the higher "on" voltage represents a 1 and the lower "off" voltage represents a "0" in binary computing. Hence, the transistor is the fundamental building block of computing. Over the years, semiconductor manufacturers set and met ambitious goals to decrease transistor size because the smaller the transistor is, the shorter the distance between source and drain and the lower the input voltage need to be. Hence a smaller transistor automatically uses less power and switches faster. This is why microelectronics manufacturers packing transistors onto chips followed an ambitious goal set by an early innovator named Gordon Moore—to double the number of transistors in each integrated circuit (IC) every 18 months. This goal—known as "Moore's Law" —is not of course a physical law but a benchmark for progress in the industry. By 2000, as the doubling time of the "Law" stretched to 2 years and longer, most manufacturers began looking for other ways to increase computer efficiency and speed as transistors were reaching both a geometrical and thermal limit of how many could be packed together in an IC.

As we detail below, the most advanced conventional (complementary conventional complementary metal oxide semiconductor (CMOS)) transistors have reached their physical limit of low-voltage operation. Without innovation, the path to ubiquitous electrification also risks significant increases in energy consumption. A new approach other than miniaturization is needed for exponential efficiency increases to prevent exponentially increasing semiconductor deployment from leading to exponentially increasing energy use. In short, without semiconductor innovation, semiconductors could become a primary contributor to increased GHG emissions rather than a key strategy to reduce them.

Microelectronics Efficiency Beyond Moore's Law

Fortunately, there are any number of ways to improve the energy efficiency of a piece of electronics that have nothing to do with transistor and these methods have been applied increasingly in recent decades as we reach the end of Moore's Law[2]. Even so, making transistors themselves more energy efficient in ways *other than* shrinking them is critical to improve the energy efficiency of general-purpose computing, which will continue to be heavily used. Furthermore, energy efficiency gains in the most fundamental building block of microelectronics *compound* with other energy efficiency improvements in computing, such as changes in architecture, optimized for specific applications.

[2] For example, there has recently been a rise in the popularity of application-specific hardware to improve energy efficiency for neural network workloads, where graphic processing units (GPUs) provide enormous gains in efficiency over generalized central processing units (CPUs) in certain tasks, and further efforts are underway to leverage specialized neural spiking hardware.

Tunnel Field Effect Transistor

As noted earlier, the operating voltage of traditional CMOS field effect transistors (FET), ubiquitous in microelectronics from the 1960's to present day, cannot be further reduced. Fortunately, the tunnel field effect transistor (TFET), relying on a different – much lower energy – principle of operation, can be used to overcome this challenge. This device, based on quantum tunneling rather than thermionic emission, was recently ranked in an IEEE analysis as the most promising new logic device, as it is projected to improve transistor energy efficiency by a factor of 10 (IEEE 2020).

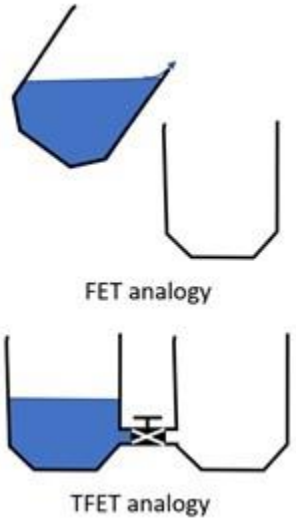

Figure 3. Buckets of water analogy for FET (top) and TFET (bottom).

The improvement in energy efficiency can be explained using an analogy of moving water between two buckets (Figure 3). Applying voltage to a FET is akin to tipping the bucket, where once some threshold angle (or for the transistor, a threshold voltage) is reached, water begins to spill out of the first bucket and into the second, allowing current to flow through the FET. In the mid-2000s, FETs began operating at such a low voltage that they behaved like a nearly full bucket. If you decreased the threshold voltage any further, as you went to pour from the bucket, fluctuations, such as from an unsteady hand, would cause undesired flow of water from the bucket. In the case of a transistor, the undesired random fluctuations that cause the current to flow (i.e., leakage current) are due to thermal energy. Continuing the bucket-water analogy, the TFET operates on a different principle entirely – it is like a pipe that connects the two buckets (Figure 3 bottom). The voltage toggles the valve, causing water (or current) to flow.

A complete explanation of operating principles of a TFET requires the language of solid-state physics. The FET has two pools of electrons sitting at the bottom of a pair of potential energy wells (Figure 4a). The voltage produced by the FET in the "on" position brings down the height of the potential hill that separates them, until electrons flow to the well that is lower in potential energy. To have a low leakage current when not in use (the "off" state), the potential hill needs to be sufficiently tall compared to thermal energy at room temperature. From the "off" state, as the height of the potential barrier is lowered, the factor that controls the rate at which the device turns on is the thermal excitation of electrons over the hill. The rate at which the electrons can flow with respect to the applied voltage is known as the subthreshold slope. In conventional

silicon FETs, this is fundamentally limited by thermal energy fluctuations, to be 60 mV/decade shown in the chart at the right of Figure 4a. Since FETs need 6 orders of magnitude more current in their "on" state versus their "off" state, and the subthreshold slope is limited to 60 mV / decade, the minimum voltage at which the FET can operate reached its physical limit decades ago.

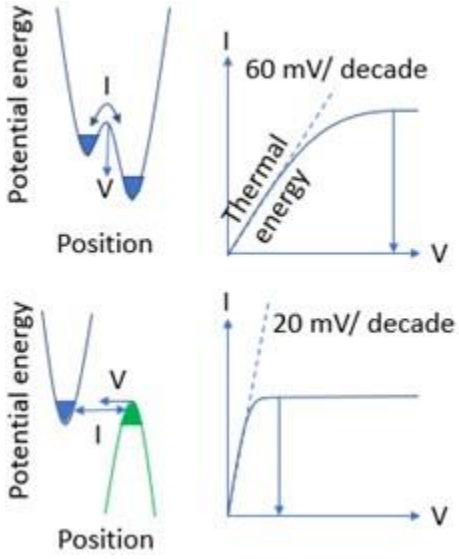

Figure 4a: (Top row) Potential energy diagram and I-V curve for a FET. (Bottom row) The same, for a TFET. Electrons are in blue; holes are in green.

The TFET, relying on band to band tunneling rather than flowing over a barrier, is not limited by the thermal energy fluctuation. As voltage is applied to the device, the gate pulls holes, a complementary charge carrier to the electron, from the drain contact towards electrons in the source contact. When these two regions are close enough, holes and electrons are able to tunnel across the potential barrier, allowing current to flow. Because thermal energy plays no direct role, the fundamental limit for subthreshold slope (20 mV/decade) comes instead from the quantum mechanical size of the charge carrier wavefunctions themselves, which are several times the atomic dimension for silicon. Their predicted current slope is three times steeper than a FET in silicon, which translates to $1/10^{th}$ the power consumption of traditional FET devices (IEEE IRDS, 2020).

Barriers to TFET Commercialization

The two critical and intertwined technical barriers that have prevented TFETs from attracting investors to commercialize the technology are the manufacturing limitations to achieve extreme energy efficiency and low current to achieve reasonable speeds. To date, TFET's subthreshold slope (slope of curves in Figure 4b) has only approached 20mV/decade when the current is very low (Ge-N-TFET in Figure 4b). In addition, the TFET's current (vertical axis) falls far short compared with a traditional MOSFET (Figure 4b). Achieving currents comparable to MOSFETs is crucial because the speed limitations for transistors are determined by their current density. Fortunately, due to application-related demand for low power (e.g., from mobile devices), TFETs likely don't need to *exceed* the speed of FETs so much as get close to it.

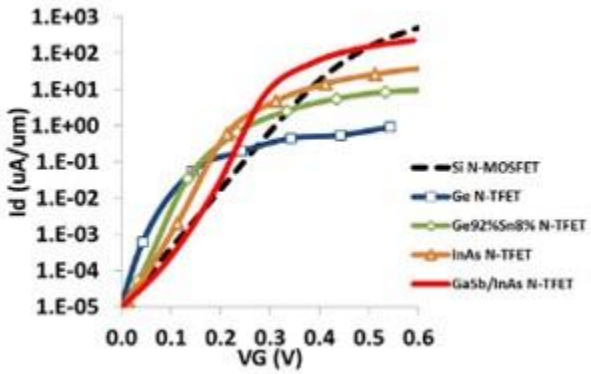

Figure 4b: Comparison of transistor drain current per unit width versus gate-to-source voltage for n-channel Si MOSFET and TFETs. All TFETs exceed the 60 mV/decade upper limit slope of MOSFET. *Source*: Avci 2014.

The limitations on current density can be understood from considering the basic geometry of the FET compared to the TFET (Figure 4c). When the transistor turns on, electrons flood from the source to the drain, in an *uninterrupted* channel. By contrast, the fundamental structure of a TFET is quite different. The device turns on by pulling the holes close to the electrons, but there is always a barrier separating the two, no matter how narrow. This *interrupted* channel, a physical barrier, will *always* support less current given the same geometry. For example, in an advanced 2D material platform, the best current densities in TFETs remain about 2 orders of magnitude smaller than those in FETs on the same platform (Li et al. 2019; Wu and Appenzeller 2019). As we detail later, Sandia's mitigation is to tailor the geometry of the transistor specifically for TFET operation – instead of having one channel, Sandia's design includes enough channels to overcome the limitation of the interrupted channel.

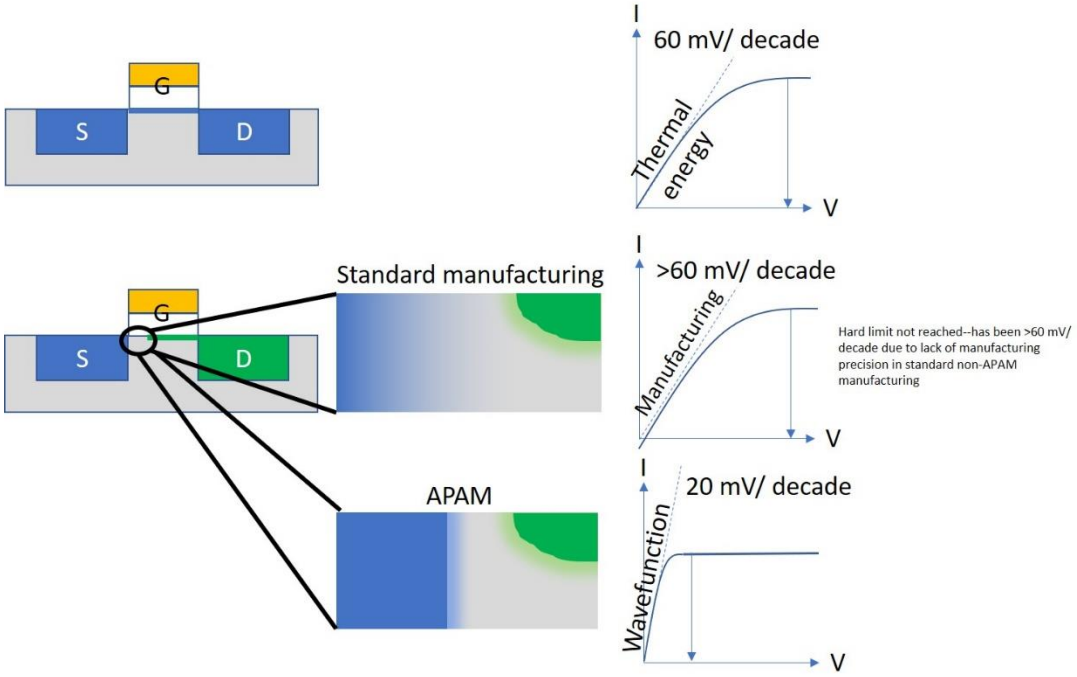

Figure 4c. Upper left shows cartoon cross section of a FET, showing the source (S), drain (D) and channel (blue line under the gate – G). Lower left shows cartoon cross section of a TFET, where a pool of holes in the drain (green) is being pulled towards the electrons in the source (blue). Middle upper close-up of the TFET near the source, with a non-precise non-APAM diffuse profile, Middle lower APAM TEFT with an abrupt doping profile In the APAM TFET, the size of the wavefunctions --shown as the halo around the source and gated holes—it what sets the lower limit on the voltage at a much steeper 20mV/decade

TFET's theoretical energy efficiency improvement over the FET has not been achieved in practice due to limitations in standard manufacturing. This can be understood by taking a closer look at what happens near the source contact, shown in the middle of Figure 4c. As the TFET is turned on, the gate pulls holes from the drain contact towards the source contact. If the boundaries of both are atomically sharp, the current versus voltage plot would be incredibly steep, leading to a subthreshold slope of 20 mV/decade as shown in the chart on the bottom right. In practice, the sharpness of the holes pulled in by the gate is set by the *size of the wave-function*, while the sharpness of the electrons is set by how the source is manufactured. The source is created by adding arsenic or phosphorus dopants to silicon at elevated temperatures, which electrically activates the dopants. However, these temperatures also make the edge of the doping profile diffuse, losing the sharp dopant interface necessary to achieve the 20 mV/decade. Consequently, high temperature dopant activation causes those TFETs with the highest current densities to typically have worse subthreshold slope than conventional FETs as shown in Figure 4b. Sandia National Laboratories has developed an APAM process that makes atomically abrupt doping profiles at moderate temperatures to improve subthreshold slope while maintaining high current densities.

Atomically Precise Advanced Manufacturing

Today, Atomically Precise Advanced Manufacturing (APAM) with Si is synonymous with hydrogen depassivation lithography (HDL). HDL, first conceived of in the 1990s by Lyding, has now demonstrated the ability to use a scanning tunnelling microscope (STM) (Figure 5) to place dopant atoms in Si for research in quantum devices and other nano electronics. HDL's low throughput restricts its current implementation to research into new devices. Furthermore, it is currently limited to a single mask material and a few substrates (Si and Ge so far). However, these limitations are being actively addressed at Sandia and elsewhere. AMO has sponsored research to scale up this technique via arrays of microelectro-mechanical systems (MEMS)-based STM scanners and distributed local control which can reach massively parallel levels (millions of tips on a 300mm wafer). Even so, while useful for low volume products, HDL will not be directly useful for consumer electronics. Instead, Sandia has shown that oxide and nitride masks, commonly used in semiconductor manufacturing today, are acceptable alternatives when atomic precision in the lateral direction is not required, as with Sandia's vertical TFET.

APAM works by reacting simple dopant precursor molecules, like phosphine, which contains phosphorus, into the clean surface of silicon. The chemical reaction of phosphine with the silicon surface produces an electrically active phosphorus donor which can be kept in place by limiting any subsequent processing to modest temperatures. The reaction can be templated to occur into select parts of the surface by masking the reaction with hydrogen, which has been used to create transistors as small as a single phosphorus atom, or thin films used in

semiconductor manufacturing, which could be used as the basis for a high-throughput process in the future.

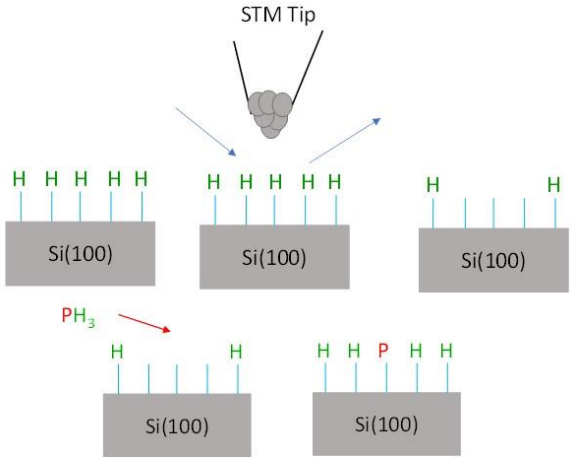

Figure 5: General flow diagram of HDL with selective phosphorous doping. After selectively plucking out hydrogen atoms, creating patterns of reactive dangling bonds, phosphine can be flowed and reacted with the dangling bond to create a Si-Phosphorous bond.

APAM TFET

AMO has recently invested in a Sandia seedling project to demonstrate a proof-of-principle TFET made using APAM to place dopants into silicon with atomic-scale abruptness, and at much higher densities than other techniques. Combined, these qualities can be leveraged to overcome both the current and the slope limitations in contemporary TFETs discussed above, helping realize the TFET's promise for energy efficiency, while providing a route to achieve improvements in current density.

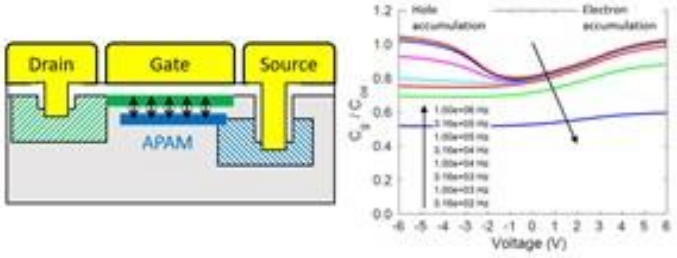

Figure 6. (left) APAM TFET. Donor implant is shown as blue striped region. APAM layer is shown in blue. Hole-type silicide is shown as green striped region. Gate-induced hole layer is shown in green. (right) C-V curve showing that a hole layer can be brought over the APAM layer at a distance where tunneling between the two is expected.

Sandia's proposed APAM TFET is shown in Figure 6. This device has a fundamentally different geometry than the other transistors discussed earlier in that it is vertical. The APAM layer is an ultra-doped sheet that constitutes the bottom layer of the transistor. The top layer is a layer of holes that the gate pulls in from the drain electrode. Tunneling occurs between this surface hole layer and the electrons in the buried APAM layer. The abruptness of the APAM doped layer is technologically simple to maintain in the vertical direction by leveraging decades-old silicon growth techniques, which define the tunneling gap. The vertical geometry effectively creates many parallel tunneling channels, boosting the total current of the device.

The manufacturing challenges in making this device are 1) a process to make the gate and drain while 2) leaving the APAM layer intact, and 3) making an independent contact to the buried APAM layer. Sandia has recently demonstrated overcoming all three of these device challenges independently. For example, the data in Figure 6 shows the capacitance between a gate and a buried APAM layer. This capacitance is high when the gate accumulates a layer of holes or electrons above the APAM layer, and it falls when that layer is depleted. In samples without an APAM layer, the capacitance at depletion is much lower. Simulations of these data further confirm that the APAM layer has not diffused but remained abrupt. In summary, the gate is able to accumulate a hole layer, as needed by the TFET, at a distance of 10 nm above a buried APAM layer, sufficient for tunneling. Incorporation of all three components –the surface drain contact and the leakage-free contact to the APAM layer – into the world's first APAM TFET is anticipated soon. These should enable the first device-informed modeling estimates of the subthreshold slope of an APAM TFET in practice, along with a rule-of-thumb for the current density.

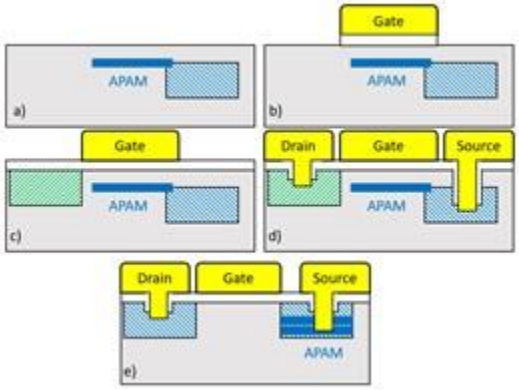

Figure 7. APAM TFET process flow. First, an ion implant is made to form the source contact, and APAM is executed on that surface to create the buried APAM electrode. Subsequently, the high-κ/metal gate is deposited on the APAM layer (b), followed by surface hole silicide formation (c). Finally, independent contacts are made to the buried APAM layer (d). (e) FET where APAM has been employed in the source contact to reduce metal-semiconductor contract resistance.

While the seedling project does not have access to state-of-the-art manufacturing that will be required for an ultimate demonstration of the speed and energy-efficiency of a microelectronic chip, the methods being used to manufacture the proof-of-principle devices are those found in modern semiconductor manufacturing, with one notable exception. Semiconductor manufacturing proceeds from high-temperature steps to lower-temperature steps, essentially freezing in successive steps of processing. The device of Figure 7 is built vertically, as shown in Figure 7, starting with a high-temperature ion implantation and activation to define the source contact. An APAM layer is then made in contact with the source contact, and encapsulated in silicon. These steps are essentially placing APAM in the middle of the manufacturing process, at a moderate temperature. Afterwards, at lower temperatures, a high-κ/metal gate is deposited over the APAM layer, a silicide is formed at the surface to source holes to the channel, and finally an electrically isolated contact is made to the buried layer. As part of another project at Sandia, APAM has been discovered to generally fit between the high-

temperature steps of so-called front-end-of-line manufacturing and the low-temperature steps of so-called back-end-of-line manufacturing.

For high volume manufacturing, each of the steps in the workflow in Figure 7 need to be accomplished by patterning a wafer with photolithography and selectively depositing a film, or etching a uniformly deposited film. Standard lithography techniques, using a photomask and a polymer resist, can be used for the ion implanted source, metal and oxide of the gate, the metal silicide for the drain, and subsequent contacting. As mentioned earlier, Sandia has demonstrated that the same masking techniques can be used to define the APAM layer as well. The vertical TFET does not require atomic precision in the lateral direction, making the reduced resolution of photolithographically-defined oxide and nitride masks an acceptable compromise for high-throughput manufacturing. Notably, this also means that the resultant transistor can be manufacturing not just with leading edge 5nm node technologies (now only found in S.E. Asia), but also legacy technologies such as the 350nm facility at Sandia and numerous other fabs throughout the United States.

The one missing step is a tool that can accomplish surface cleaning, phosphine doping, and silicon capping at high throughput, and on the wafer scale. Such a tool does not yet exist, although attempts are being made to identify a commercial driver, as shown in Figure 7 (d). The size of a modern transistor is not actually set by the size of the channel, but rather by the size of the contacts. As transistors have shrunk, the channel resistance decreases, but the contact resistance increases, and so the contact sizes have saturated recently. APAM, through ultra-doping, may reduce the contact potential between metal and semiconductors. Incorporation of APAM into source and drain contacts on FETs could thus decrease parasitic effects, and enable further reductions in contact size. If such a tool can be developed for high-volume manufacturing of FET contacts, the same tool can be repurposed for the TFET process flow, enabling a route to manufacturing for the APAM TFET.

Future research needs for extreme energy efficiency in microelectronics

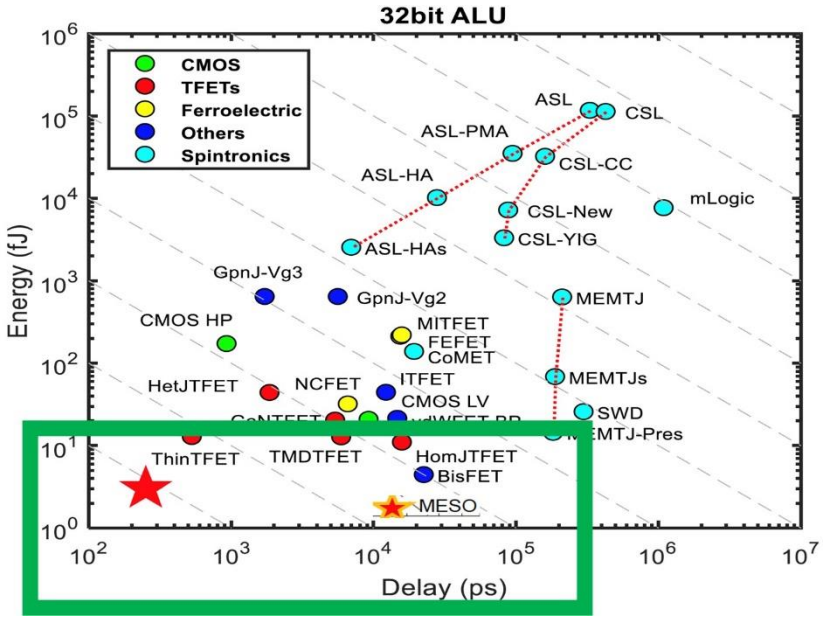

Figure 8. The green rectangle shows the "preferred corner" for an extremely energy efficient logic transistor. Technologies that are competitive with TFET for key applications include Ferroelectric gate transistors (FeFET and negative-capacitance NCFET—Note that there also is a FeTFET!) and Magneto-electric spin-orbit (MESO) logic. *Source:* Pan 2017.

AMO's second workshop on Ultra-precise control for ultra-efficient devices (Figure 8) showed that several other types of transistors offer the potential for extreme energy efficiency in key applications with the strongest growth. Figure 8 shows that ferroelectric and spintronic transistors—both of which also are supported by AMO's current research portfolio—also are in the running for an extreme energy efficiency transistor (DOE/AMO 2021c). In addition to RDD&D on more efficient transistors and other devices (and related process and materials innovation) in the coming year, AMO also will explore other, potentially very large sources of energy efficiency gains that could benefit from manufacturing RDD&D. AMO will do this through workshops, Requests for Information (RFI), and focused roundtable discussions. Future workshop topics include a) analog and neuromorphic architectures that overcome the compute and memory divide and b) 3D monolithic and heterogeneous integration.

As these portfolio investigations continue, AMO will also work with Sandia, other participants in its microelectronics research portfolio, and industrial representatives, such as the Semiconductor Research Corporation (SRC), to identify near term urgent commercialization opportunities for the portfolio's manufacturing innovations related to near term performance gains needed by tool makers that would benefit from scale up of APAM technologies such as Sandia's deposition-based APAM ultra-doping for abrupt doping profiles. Once toolmakers commercialize tools for mass producing abrupt doping profiles, it will lay the groundwork for fabrication of next generation extreme energy efficient transistors and other microelectronics made from them. The TFET appears to be one of the best candidates for energy efficiency in general purpose computing and the TFET can be used in conjunction with other extreme energy efficiency manufacturing solutions under development at AMO. Thus, should Sandia's research or other research in AMO's APAM portfolio be successful and tool maker(s) commercialize the technology, it would set the stage for an industry–government RDD&D partnership to enable extremely energy efficient TFETs to be mass manufactured in the United States—providing extreme energy efficiency product to the planet, and good-paying jobs for Americans.

References

BEA (Bureau of Economic Analysis). 2020. *Gross Domestic Product by Industry: Third Quarter 2020*. Washington, DC: BEA.

BLS (Bureau of Labor Statistics). 2021. "Industries at a Glance: Manufacturing: NAICS 21-33." Washington, DC: BLS. e

DOE (Department of Energy). 2015. *Quadrennial Technology Review: Chapter 6: Innovating Clean Energy Technologies in Advanced Manufacturing*. Washington, DC: DOE. www.energy.gov/sites/default/files/2017/03/f34/qtr-2015-chapter6.pdf

DOE/AMO (Advanced Manufacturing Office). 2021a. "Vision, Missions, and Goals." Washington, DC: AMO. www.energy.gov/eere/amo/vision-mission-and-goals

———. 2021b. "Report on First Workshop on Semiconductor R&D for Energy Efficiency: Integrated Sensor Systems" held Jan 25-26 virtually. Washington, DC: AMO. Forthcoming

———. 2021c. "Report on Second Workshop on Semiconductor R&D for Energy Efficiency: Ultra Precise Control for Ultra Efficient Devices" held April 21-23 2021 virtually. Washington, DC: AMO. Forthcoming

———. 2021d Industrial Decarbonization Roadmap 2021. Forthcoming

DOE/BES (U.S Department of Energy, Office of Basic Energy Sciences) 2021. Basic Research Needs for Transformative Manufacturing. https://science.osti.gov/-/media/bes/pdf/reports/2019/BRN_Microelectronics_rpt.pdf

EIA (Energy Information Administration). 2020a. "Annual Energy Review." www.eia.gov/totalenergy/data/annual/

———. 2020b. *Annual Energy Outlook 2021*. www.eia.gov/outlooks/aeo/pdf/AEO_Narrative_2021.pdf

EPA (Environmental Protection Agency). 2021. "Sources of Greenhouse Gas Emissions." Washington, DC: EPA. www.epa.gov/ghgemissions/sources-greenhouse-gas-emissions

Granholm, J. 2021. "Deploying the Clean Energy Revolution." Washington, DC: DOE. www.energy.gov/articles/deploying-clean-energy-revolution

IEEE (The Institute of Electrical and Electronics Engineers). 2020. *The International Roadmap for Devices and Systems: 2020 Edition Beyond CMOS*. Piscataway, NJ: IEEE.

Kaarsberg, T., E. Hopson, and K. Clay. 2004. *Technologies to Halve U.S Energy Use in a Decade* ID # 312 presented August 24, 2004 at the American Council for an Energy Efficient Economy (ACEEE) 2004 Summer Study on Energy Efficiency in Buildings, Pacific Grove, CA (US).

Kerry, J. 2021. *U.S. Climate Pledge on Earth Day 2021*. Washington, DC: The White House. www.whitehouse.gov.

Li, X., et al 2019. "High-speed black phosphorus field-effect transistors approaching ballistic limit." *Science Advances* 5 (6).

Nadel, S., and L. Ungar. 2019. "Halfway There: Energy Efficiency Can Cut Energy Use and Greenhouse Gas Emissions in Half by 2050." Washington, DC: American Council for an Energy-Efficient Economy. aceee.org/research-report/u1907.

Occo, R., Ken Somers, Eveline Speelman, and Maaike Witteveen. 2020. “Plugging in: What electrification can do for industry.” McKinsey and Company. www.mckinsey.com/industries/electric-power-and-natural-gas/our-insights/plugging-in-what-electrification-can-do-for-industry

Pan, C. and Azad Naeemi. 2017. “Beyond-CMOS Non-Boolean Logic Benchmarking: Insights and Future Directions.” *Proceedings of the Conference on Design, Automation & Test in Europe*. 133 – 138

Roberts, D. “The key to tackling climate change: electrify everything.” Oct. 27, 2017. https://www.vox.com/2016/9/19/12938086/electrify-everything

SRC/SIA (Semiconductor Research Corporation/Semiconductor Industry Association). 2021. *The Decadal Plan for Semiconductor: Full Report.* Durham, NC: SRC. www.src.org/about/decadal-plan/

Avci, Uygar E., Daniel H. Morris, and Ian A. Young. 2014. “Tunnel Field-Effect Transistors: Prospects and Challenges,” *Journal of the Electron Devices Society* 3(3): 88 – 95

Wu, P and J. Appenzeller. 2019. “Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor with Record High ON-Currents.” *IEEE Electron Device Letters* 40 (6): 981 – 984.