Power Factor Requirements for Electronic Loads in California

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ABSTRACT

Nonlinear loads, which are normally powered by ac-dc switching power supplies, are typical in a wide range of electronic devices, such as computers, monitors, televisions, printers, fax machines, copiers, audio equipment, and telecommunications equipment. Residential and commercial miscellaneous loads, which include consumer electronics, are the fastest growing segment of household energy use in the United States.

Power factor is a measure of the efficiency with which a load uses the current supplied to it. Typical power factors are shown in Figure 6.The nonlinear loads described above have a poor power factor, and thus draw more current than required for the DC load on their output. This is because of harmonics that are inherent in the power supply current, due to their design. However, this can be corrected using power factor correction (PFC) circuitry at the front end of the power supply – an approach required in Europe and Japan for high wattage devices. In so doing, the current flowing in the building wiring is reduced, and this in turn can reduce heating effects in the wiring from that current. While efforts are underway to improve power supply efficiency through standardized test methods, voluntary labeling programs, and mandatory efficiency standards, parallel discussions are addressing whether or not to require PFC in the high efficiency designs. Without any harmonic compensation, the highly distorted load currents of computer workstations, such as those shown in Figure 1, as well as other electronic loads, can lead to losses in the building wiring that are much higher than for undistorted load current.

This paper describes a project designed to definitively determine the energy savings potential in building distribution wiring from power factor correction in various end use electronic products, and recommend appropriate Title 20 requirements for securing those savings cost effectively. In addition, there are other, non-energy benefits associated with PFC (reduction of harmonics) that are of interest. The final conclusion shows that the opportunities for energy savings are not as large as previously thought, but are still compelling.

Introduction

There are three major types of electric loads in commercial and residential buildings—resistive, reactive, and nonlinear. Resistive loads are those from incandescent lamps and electric resistance heaters. Reactive loads are typically inductive, such as electric motors that might be found in pumps and compressors. These loads draw current that is out of phase with the source voltage, which reduces the amount of active power transferred to the load. Nonlinear loads, which are normally powered by ac-dc switching power supplies, are typical in a wide range of electronic devices, such as computers, monitors, televisions, printers, fax machines, copiers, audio equipment, and telecommunications equipment. As interest in cost effective opportunities to reduce electrical consumption has grown, attention is increasingly turning to these nonlinear loads, which include most electronic products previously classified as “miscellaneous load” or “plug load.” Residential and commercial miscellaneous loads, which include consumer electronics, are the fastest growing segment of household energy use in the United States. While the relative energy intensity of applications such as heating and cooling is declining, the DOE’s

Annual Energy Outlook forecasts that the intensity of residential and commercial miscellaneous end-uses, as defined in the 2007 Annual Outlook, will increase significantly by 2030.

The following is an overview of harmonics in building power systems, to establish the causes and effects. After this, the energy savings potential will be explored.

Most harmonic currents in commmercial systems are caused by nonlinear loads, that is, loads that draw currents whose frequencies differ from the frequency of the source. Many electronic devices are nonlinear loads because they use solid state rectifiers at their inputs and filter capacitors after the rectifiers. An example of this type of circuit is a personal computer power supply, as shown in Figure 1.

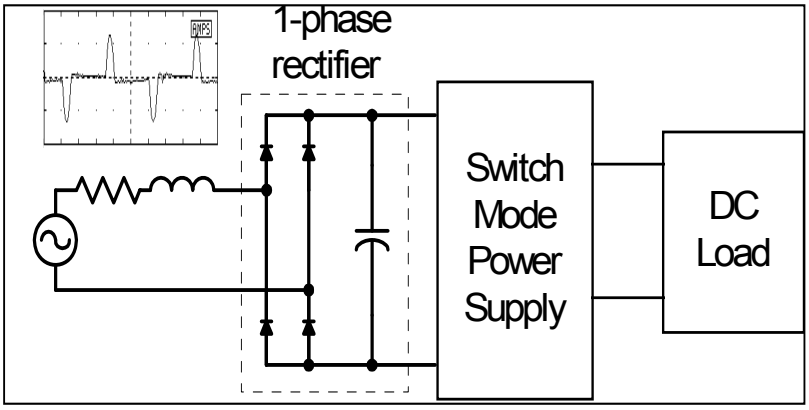

Figure 1. PC power supply circuit diagram.

Solid state rectifiers inherently draw current in pulses, when the AC line voltage is higher than the voltage across the filter capacitor used with the rectifier. This pulsed current is very rich in harmonics, as seen in Figure 2. The harmonic spectrum plot shows the presence of odd harmonics, with relatively large magnitudes at the lower frequencies. As the frequency increases, the magnitudes decrease.

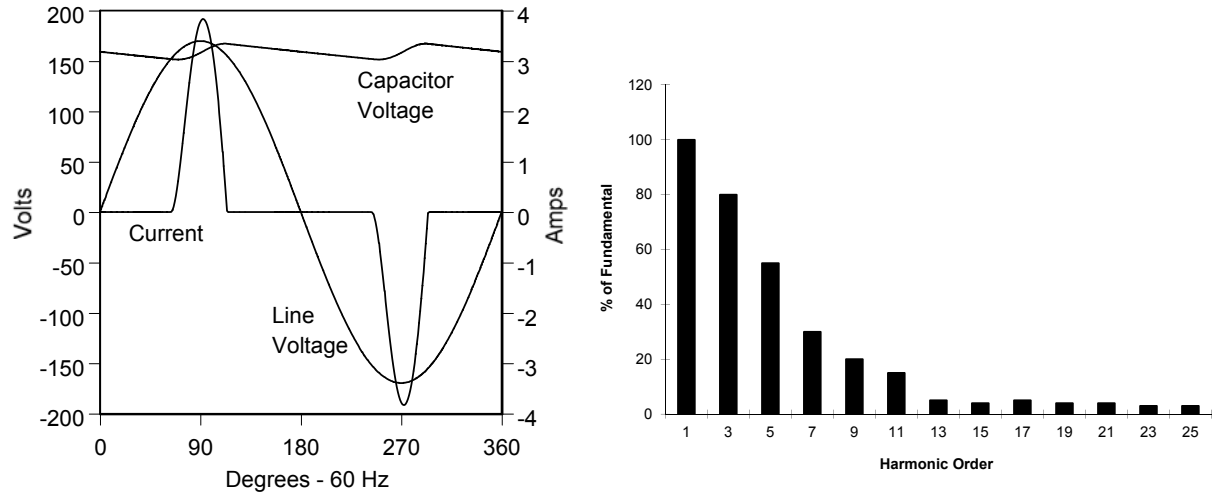

Figure 0. PC power supply current and spectrum.

The PC power supply is only one of many possible harmonic producers in the 120-volt range. Other loads that inject harmonic currents include office equipment for communications,

printing and copying and lighting with high efficiency electronic ballasts. Nonlinear loads in the 480 V range include adjustable-speed drives (ASDs) for HVAC, larger computers, uninterruptible power supplies, and 277-V lighting.

Problems Related to Harmonics

Harmonics result in an increase in the rms value of current, which increases line losses (heating in wiring, given by I^2R, where I is the rms current, and R is the resistance in the wire).

The rms value of the current is given by

$$I = \sqrt{\sum_{h=1}^{\infty} I_h^{\,2}} = \sqrt{I_1^{\,2} + I_2^{\,2} + I_3^{\,2} + \ldots}$$

Where I is the total rms current,
h is the harmonic number,
I_1, I_2, etc, are the current components at the first and second harmonic, etc
I_h is the current component at the h^{th} harmonic

Since the rms value of the current is higher when THD is higher, the heating effect associated with I^2R losses is higher than it would otherwise be. (I^2R is the value of the power consumed in the wiring, where I is the current and R is the resistance in the wire). These losses manifest themselves in a number of specific ways:

- Heating effects in phase conductors as well as neutrals
- Heating in 3-phase, dry-type transformers
- Harmonic voltage related heating in other equipment, such as motors
- Harmonic voltage stress on system capacitors and equipment capacitors
- Resonance with power-factor-correction capacitors
- Voltage distortion at the point of common coupling

Wiring I^2R losses will vary, depending on the length of the line segments, the amount of load traveling through them, and the nature of the load. The distorted current with low power factor leads to relatively higher losses-per-watt of connected load. Without any harmonic compensation, the highly distorted load currents of computer workstations, such as those shown in Figure 1, as well as other electronic loads, can lead to losses in the building wiring that are much higher than for undistorted load current. Also, the effectiveness of harmonic elimination methods will be highly dependent on their locations in the building wiring. Usually, the best location for harmonic filters is at the offending load. Power factor correction (PFC) circuits can be added to the front end of nonlinear devices to eliminate their harmonic contribution to the power system.

Transformer losses are well defined, with derating for harmonics covered in ANSI C57.110. Losses are divided between load and no-load losses. The load losses include I^2R losses and stray losses. It is the stray losses that are most affected by the harmonic content of the current waveform. There are eddy-current losses that cause heating in many transformer parts,

but it is the heating in the windings that is of most interest. This heating is proportional to the square of the load current and the square of the frequency, which leads to the notion of a *K factor* promoted by some transformer manufacturers. The K-factor serves as an indication of the additional eddy current heating in the winding. This K factor is given by

$$K = \frac{\sum I_h^2 h^2}{\sum I_h^2}$$

Where h is the harmonic number,
I_h is the h^{th} harmonic component of the current.

The derated transformer current is given by

$$I_{RMS} = \sqrt{\frac{1 + P_{EC-R}}{1 + K * P_{EC-R}}}$$

Where P_{EC-R} represents the rated eddy-current losses for that transformer design.

This K factor takes into account the additional eddy current heating in the windings due to the harmonic components of the nonlinear current.

Power Factor Correction

One of the impacts of harmonic content in load current is an increase in the rms value of the current, as shown before.

This results in additional heating of the building wiring and transformers. Since the harmonic content also manifests itself in the power factor, power factor can be used as a measure of the level of harmonics as well as a measure of the losses they cause in the power system. These problems can be avoided by the manufacturer through the use of a power factor correction circuit, which effectively removes the harmonics from the power supply current.

Previous work for the CEC showed that the use of PFC power supplies inherently reduces the current in the building wiring and thus reduces the heating or I^2R losses associated with the harmonic-rich currents. It was of great interest to study the topic and develop an understanding of what typical energy savings might be achieved in the building distribution wiring through such an approach. In order to do this, a model was developed and lab tests performed to establish some typical values of possible energy savings. In addition, there are other, non-energy benefits associated with PFC (reduction of harmonics) that are of interest. Both the results of the tests and calculations and the non-energy benefits of interest are outlined in the following sections.

Methodology: Laboratory Tests for Desktop Computers

Lab testing was performed to ensure that the theoretical effects of PFC on system wiring losses were reasonable and achievable. In order to determine the energy savings due to PFC loads, the following procedure was adopted. The test was conducted in an environment where the

source voltage could be controlled. A total of 24 computer power supplies were chosen for this test—8 units without PFC, (referred to as NPFC), 8 PFC units and 8 80 PLUS units. The 80+ PLUS units are power supplies that achieve an efficiency over 80% at 20%, 50% and 100% load and include power factor correction. Non-80 PLUS units have efficiencies between 60 and 80%. Each of the 24 power supplies had identical 200-W output power ratings. All the power supplies were loaded identically; that is, each power supply was loaded with constant resistors on the dc side having total dc power output of 97 W. The 12-V bus was loaded to 72 W (2-ohm resistor) and the 5-V bus was loaded to 25 W (1-ohm resistor). The tests were set up as shown in the diagram below (Figure 4).

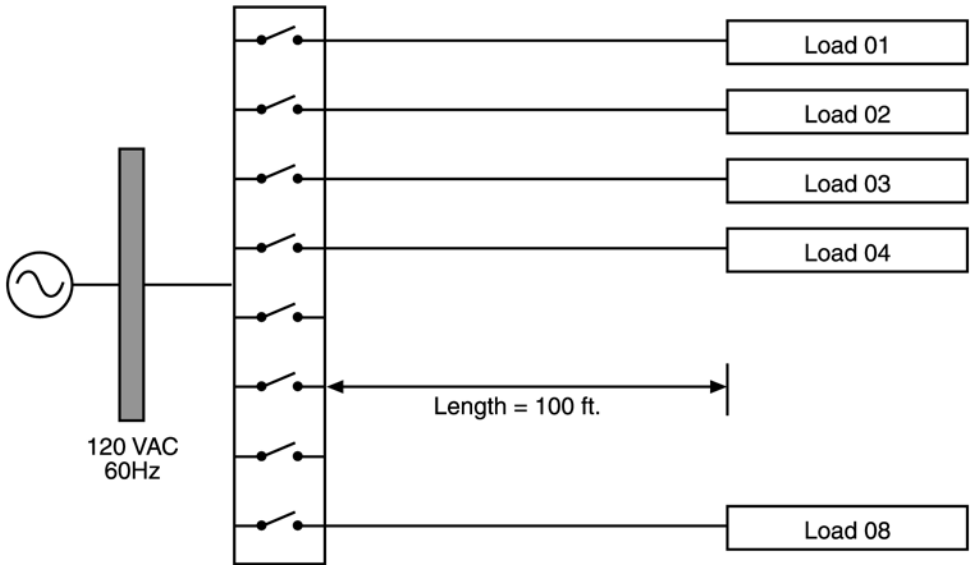

Figure 2. Wiring diagram for cable loss tests.

Measurements were taken first using 8 power supplies without PFC and then again using 8 PFC-equipped power supplies, then finally with 8 80 PLUS power supplies.

Test Results

Test results indicated that while the change in wiring losses is small, there are reductions in the power consumed by the power supply itself.

The loads were carefully controlled to ensure that the output power was the same in all cases. As the line current was reduced, the power factor increased, automatically reducing the power consumed.

In a linear system,

$$P = V_{RMS} I_{RMS} \cos\theta$$

Where θ is the angle between the voltage and the current.

In systems with inductive loads, there is a displacement between the voltage and current given by this angle θ. The cos of this angle is known as the displacement power factor since it depends only on the angle between voltage and current. There is a term known as true power factor, which is equal to the ratio of real to apparent power.

If there is no distortion, true power factor is equal to displacement power factor. In the presence of distortion, however, these two are no longer equal and must be studied further.

The above equation still holds true, although it is more correct to write it as follows:

$$P = V_{RMS} I_{RMS} PF_{TRUE}$$

Where

$$PF_{TRUE} = \frac{PF_{DISP}}{\sqrt{1 + THD_I{}^2}}$$

However the single-phase power supplies of interest here are a special case in which the angle between the voltage and current is 0, making the cosine equal to unity. Therefore, any reduction in power factor is due to the presence of harmonic distortion, and so power factor is typically directly related to harmonic distortion in power supplies.

One result is that the benefits, or savings, from using 80 PLUS power supplies can be attributed to three effects:

1. **Savings by virtue of more efficient power supply.**
   This is the original intent of using 80 PLUS power supplies, and is the most significant effect.
2. **Indirect savings in wiring due to lower current requirement of the more efficient power supply.**
   This is a side effect of high efficiency loads, and while it is relatively small, it is still real and measurable (and has usually been ignored in past analyses).
3. **Indirect savings in wiring due to power factor correction.**
   This is a known and measurable effect of PFC loads, larger than the indirect savings from higher efficiency and a significant added savings of energy.

The results of the testing and modeling are shown in Figure 4, where the savings from the efficient power supply are normalized to 100%. This allows the magnitude of the other effects to be compared. A major result from these findings was that EPA's Energy Star program added a power factor correction requirement to the desktop computer power supply efficiency specification in 2007. This specification was Energy Star Computer Power Supply Specification Version 4.

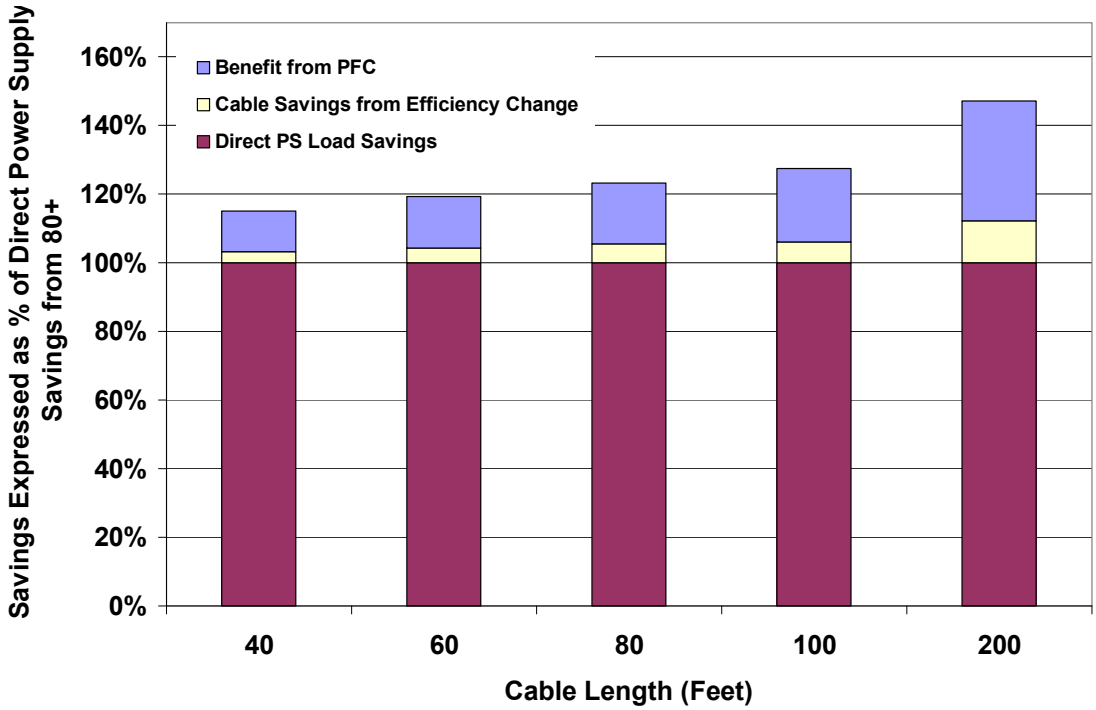

Figure 4. Comparison of savings from PFC and efficiency improvement in percent.

These are conservative estimates, because they neglect other loading that might be on the same cable, such as laser printers, copiers, and monitors. Because losses are proportional to the square of the rms current, the incremental change in losses is twice the present loading level.

$$\frac{dP_C}{dI} = \frac{dI^2 R_{CABLE}}{dI} = 2IR_{CABLE}$$

For example, if the load were 10 A, and were reduced by 1 A, the difference in losses (savings) would be

$$10^2 R - 9^2 R = 19R \text{ watts}$$

But if the load were 25 A, and were reduced by 1 A, the savings would be

$$25^2 R - 24^2 R = 49R \text{ watts.}$$

This finding is particularly noteworthy as the share of nonlinear loads continues to grow in commercial buildings.

Current Project

Building on the findings of the previous CEC work, the current project was designed to do a similar analysis for ALL electronic loads. The research question to be answered is whether PFC requirements might garner enough energy savings to warrant Title 20 regulation.

Because the harmonic wiring losses depend on building wiring topology, it was necessary to determine typical topologies for residential and commercial buildings. To narrow down the variety in residential and commercial buildings, buildings with high annual energy use[1] and well-known loads were selected.

Floor space was used as the criteria to narrow down residential to three representative sizes:

- Small 800-1000 square feet (typically 2 bedroom, 1 bath with dining space in kitchen)
- Medium 1500-2000 square feet (typically 3 bedroom, 2 bath with separated dining space)
- Large 2500-3000 square feet (typically 4 bedroom, 3 bath with formal dining space)

These categories were chosen because the National Electric Code (NEC) is driven by floor space.

A sample of homes in California were chosen to physically measure the loads on individual branch circuits. The primary reasons for these measurements were to validate the load testing in the laboratory, and to determine some idea of typical coincidence of load, since it can affect the savings achieved, as described above.

Lab tests revealed power factor levels for various electronic loads, which will be used in the analysis. A sample of these values are shown in Figure 6.

[1] Based on CA stock estimates and energy intensity per square foot

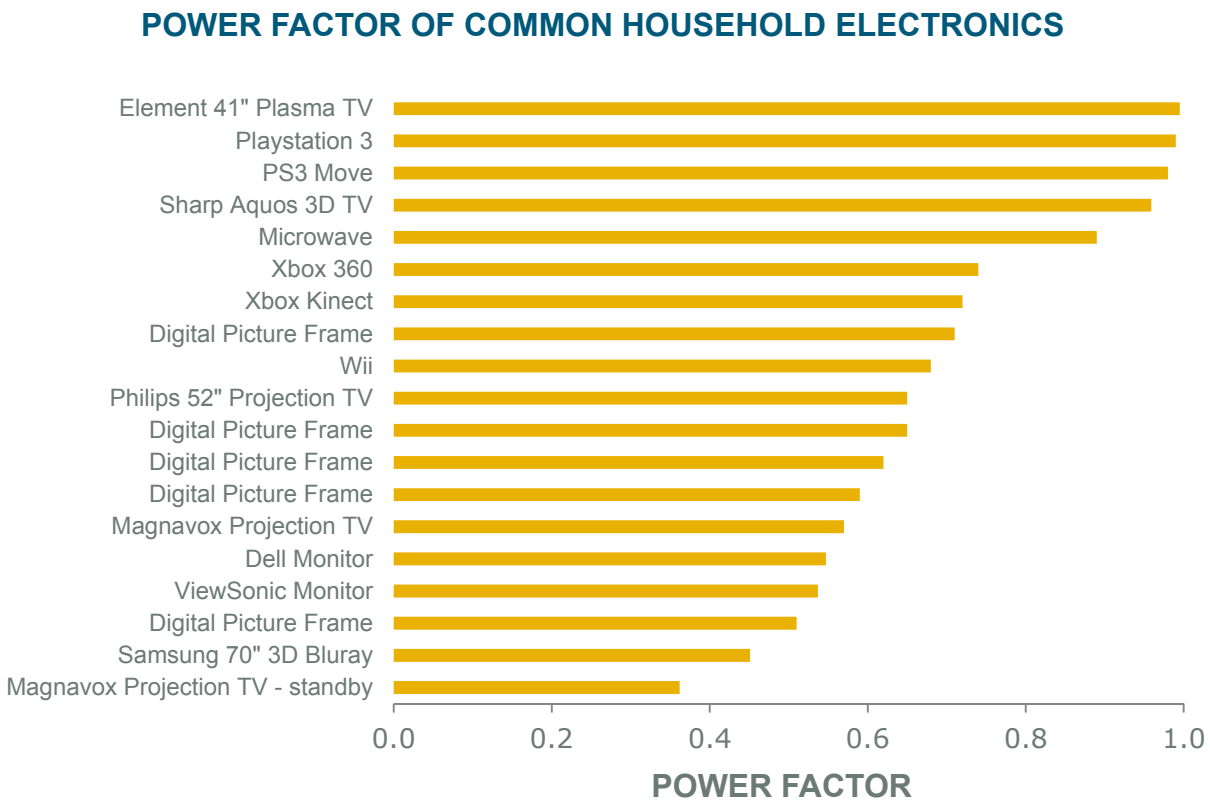

Figure 6. Measured power factor of selected electronic loads.

In this scenario, the analysis is simplified by the fact that harmonic mitigation is the only change. With the power supply work, the devices were more efficient which led to three energy savings mechanisms. Here, the only means of achieving energy savings is through the reduction/elimination of harmonic distortion, which reduces the RMS value of the current. Therefore, to model the system, it is only necessary to use the current spectrum measured in the lab, calculate the losses using the RMS value measured, applying the coincidence of other loads.

To compare, the same scenario is adjusted by removing the harmonic components of the current. This is accomplished by simply using the fundamental component of the current as the rms value. The energy savings is then calculated as the difference between the two scenarios.

Previous projections were that energy savings from power factor correction could be just under 2% of all plug loads. This equates to approximately 1.4 Billion kWh per year for the state of California. Stakeholder outreach efforts have shown strong support for inclusion of PFC requirements for electronic loads in California. This project, however, through more rigorous analysis, demonstrated that those projections were somewhat optimistic, and some adjustments have been made to the projected energy savings.

Conclusions

Through the process of determining the savings potential of implementing PFC in electronic devices across California, there were several interesting discoveries that are of note.

1. The amount of savings in the residential sector is much smaller than previously estimated. As a result, power factor correction in residential appliances is not likely to be

a cost-effective option for legislative efforts, except for large, relatively power hungry devices like televisions. However, commercial savings are more easily and cost effectively realized, and should still be considered as a viable option for codes and standards bodies such as Title 20.

2. Homeowners that participated in the field study were turning their devices (computers, laptops, computer monitors) off when not in use rather than leaving them on to idle for significant periods of time. Previously, estimates to determine energy consumption in residential applications of office equipment assumed a device would be turned on, used for a period of time, and then left on to sit idle while not it use. Data collected in the field shows that in the twenty-two homes surveyed, the computers and laptops were actually turned off when they were not in use, and the duty cycle was between 20% and 40%.
3. Since the savings potential of implementing PFC increases with higher currents, and kitchens typically house the appliances with some of the highest currents (coffee makers, toasters, microwaves, etc.), it was expected that the kitchen could provide a reduction in energy losses from PFC. However, kitchens do not present much of a savings opportunity in most cases. This is due to almost every appliance in a kitchen being either power factor corrected, a resistive load, or a motor load (such as a refrigerator). Resistive loads (toaster, coffee maker, etc.) already have a PF of 1 and do not draw a current with harmonic content so there is no room for improvement in these devices. Motor loads, such as refrigerators or dishwashers, may have a PF less than 0.9, but it is due to displacement and not distortion. Refrigerators are primarily motor loads with the fan motors and a compressor motor, and motors do not distort the current, but rather shift it out of phase with the voltage causing displacement. This type of low power factor cannot be corrected with the removal of distortion, which is the subject of this report.

Significance

The research contained in this report can be used to inform the Title 20 rulemaking process, and increase the overall energy efficiency of California's electronic devices. Currently, improving power factor in electronic devices is a largely untapped avenue for significant energy savings. In the United States, California is the only state to regulate PF at all, and that presently only affects televisions of 100 W or higher. This work shows that there is a much greater opportunity than televisions alone.

Title 20 Impacts

EPRI measured the power factor of a number of home electronics and appliances to determine the potential impact of statewide minimum power factor standards.

With the exception of state level regulations on television power factor, no other state or federal power factor standards apply to plug loads. In California, televisions must be power factor corrected to 0.9 when they exceed 100 W during operation. Some voluntary specifications, such as the 80 Plus program and Energy Star for desktop power supplies, require specific power factor performance levels for plug loads. Many products that would benefit from improved power factor are also already subject to regulation related to other aspects of device performance.

The relative level of effort required to implement power factor correction policy was rated as high due to the diversity of products covered under potential regulations. Manufacturers from dissimilar product classes would have to be engaged and the technical implementation of

power factor correction equipment evaluated. Energy savings were seen as low, but cost effective due to low per product upgrade costs. Existing state and federal device regulations may cause preemption issues and should be further studied.

Considering the above factors, the EPRI research team developed a recommended specification that could inform Title 20 policy that would require all plug-loads larger than 50 watts to have power factors of at least 0.9 at 50 and 100 percent load. With this policy, an estimated energy savings of 241 GWh per year after full stock turnover could be achieved.

There is a research need to investigate the potential savings from PFC further, so that energy savings projections can be even more exact. In order to further refine these findings, it will be necessary to perform even more detailed load monitoring on a larger sample of both residential and commercial spaces, increasing the granularity of the data.