STRATEGIES TO IMPROVE ENERGY EFFICIENCY IN SEMICONDUCTOR MANUFACTURING

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INTRODUCTION

The global semiconductor industry is growing at an astounding rate. In the next few years, the industry is expected to invest some $169 billion to build more than 36 million square feet of clean room floor space. Electric loads in these new plants are expected to total more than 5000 MW and 40,000 GWH per year.

This paper summarizes the results of studies to identify opportunities for improved energy efficiency in the semiconductor industry. The genesis of this work came about as we observed the rapid growth of the semiconductor industry in the Pacific Northwest. Industry observers report that some $20 billion in new facilities could be built in the Northwest in the next few years, with a combined electric load in excess of 500 to 600 MW[1].

The research results reported in this paper have been supported in part by the Bonneville Power Administration, the Northwest Power Planning Council, the Oregon Office of Energy, New England Electric System and the Conservation Law Foundation of New England. With their support we interviewed numerous industry participants, reviewed key literature, and met extensively with industry engineering firms, manufacturers, vendors and suppliers of manufacturing equipment and materials, and others with interests in this industry.

Significant opportunities to improve energy efficiency in the semiconductor industry have been reported to us; perhaps 50 percent or greater aggregate improvement appears possible. Equally significant market barriers constrain the industry from achieving these savings.

Yet, because of this industry's concentration, competitiveness, and existing research consortia such as SEMATECH, we believe the substantial market barriers to energy efficiency can be addressed with carefully formulated strategies to demonstrate, document and communicate the business and technical case for advanced energy efficiency, including potential benefits in finance, manufacturing and corporate environmental performance.

This paper describes how the industry plans research and development investments, examines energy use intensities, summarizes key market barriers which constrain energy efficient design, identifies interests in the industry that may be changing energy efficiency perceptions, lists activities to move energy efficiency to a higher priority, gives examples of energy efficiency opportunities, and reviews activities planned by a coalition of Northwest interests to accelerate the adoption of energy efficient design strategies.

BACKGROUND: MOORE'S LAW AND EXPLOSIVE GROWTH OF THE INDUSTRY

Since Intel's cofounder Gordon Moore observed in the 1960s that semiconductor performance doubles every 18 months, "Moore's Law" has guided the industry's rapid growth. This growth is based on continually increasing microchip complexity and speed, while reducing cost per function. "Better, Faster, Cheaper" is industry's paradigm.

To manage the research and development and capital investment planning required to sustain rapid growth the industry created the "National Technology Roadmap for Semiconductors"[2]. Revised every three years through an industry consensus process, the Roadmap provides a 15 year R&D outline for each of the key enabling technologies. Every three years, according to the Roadmap, a new technology generation will be introduced. Each new technology generation is faster, has more transistors per unit area, and provides increased function.

Feature size reduction distinguishes each succeeding generation. This is "the physical dimension of an individual pattern element, usually expressed as minimum feature size. For example, a 0.8 micrometer process

has a minimum gate dimension of 0.8 micrometers (micron, or 10^{-6} meters)."[3] Currently the industry is building leading edge chips at .35 micron. Companies are beginning to announce production capability at .18 micron.

Smaller feature sizes require cleaner manufacturing facilities, to minimize airborne particles which can contaminate the chip surface and cause it to fail. Each defective chip reduces production process yield, and yield is a key metric which the industry tries to maximize.

As feature sizes shrink and cleanliness standards tighten, the fabrication facilities ("fabs") in which chips are manufactured have become more expensive. Their energy loads are also expected to increase, due in part to the larger volumes of air which must be filtered.

New technology generations also require production equipment, or "tools" in the industry vernacular, which can produce the feature size required. Most critical to this are the functions that create the patterns on the surface of the chip. As each feature size generation comes into commercial production, the industry continues to design next generation tool sets and fabs required to produce even finer and finer features.

Thus, the industry is continually inventing the next tool and process, and designing and building the next generation fabs to produce the latest product. Even as new plants for next generation products are built, the industry's older facilities continue to produce chips for functions in which the latest design is not required. Older fabs are retooled in some cases to update their production capability.

Because of the huge costs associated with building a new fab, capital equipment life extension is important in the industry. New chip fabrication plants can be expected to be in use for twenty years or more. The production tools may remain useful for seven to ten or more years, with some tools which are not feature size constrained having quite long useful lives.

Gordon Moore, now Chairman Emeritus of Intel, recently speculated that Moore's Law would continue for at least another twenty years, though the time between feature size generations may stretch out to four years[4]. Thus, even larger manufacturing energy loads are likely as demand for new chips increases, new generations of technology are developed every three to four years, and new clean room and production capacity is added to the existing industry base.

SEMICONDUCTOR INDUSTRY ENERGY USE AND GROWTH PROJECTIONS

In the period 1995 through the first half of 1996 the semiconductor industry announced plans to invest some $169 billion in new clean room floor space[5]. The expected U.S. share of these industry investment plans is some $56 billion to add 12.2 million square feet. To put these expected investments into context, the 1994 existing U.S. base of semiconductor clean room capacity was about 5.1 million square feet[6].

Table 1. U.S. Semiconductor Industry Fabrication Plants
Current and Projected Electric Load Summary.

Metrics	Installed Fab Capacity 1994 (N=281)	SEMATECH Benchmarks 1996 (N=3)	1Q95 - 2Q96 Announced Fabs (N=86)
Clean Room Space, 1000 Sq. Ft.	5,155[7]	513[8]	12,118[9]
Annual Electric Cost, $ Million	$406[10]	$27.8	$657
Gigawatt Hours per Year	7,469	557	13,150
Megawatts	947	71	1,668
EUI – kWh per Square Foot/Year	1,449	1,085	
EUI – Watts per Square Foot	184	138	

In Table 1 we present calculated energy use intensity data from two sources. Installed U.S. fab clean room space in 1994 was related to 1994 semiconductor energy consumption figures from the U.S. Department of Commerce. This data yielded EUI values of 1,449 kWh per square foot per year and 184 watts per square

foot. In the second source, a 1996 SEMATECH survey of facility costs in three fabs yielded 1,085 kWh per square foot and 138 watts per square foot.

We do not know the specific reasons that the EUI data are different. The SEMATECH data is a small sample that may be unrepresentative, and it is worth noting that the 1994 Fab Capacity EUIs are derived from two different data sets, which may introduce some error. Given these limitations, the similarities between the two calculated EUIs are striking. These data illustrate the magnitudes of industry energy intensity.

New semiconductor fabs exhibit large electrical demands at high load factors. For example, five new fabs valued at $6.1 billion have total connected electric loads of 201 MW, averaging 33 MW per $1 billion invested[11]. While not a scientific sample, we believe these five fabs illustrate the general trends and scale of new electric loads. In load growth calculations below this projected electrical load growth was rounded to 30 MW per $1 billion investment. Discussions with fab engineering firms and industry analysts suggest electric load factors in these facilities will be about 90 percent[12].

Table 2 shows the planned construction schedule at the time of announcement for both U.S. and Rest of World for facilities announced between January 1, 1995 ("1Q95") and June 30, 1996 ("2Q96"). We expect that semiconductor industry electrical demand will increase significantly as new fab capacity is built. As Table 2 illustrates, for fabs announced 1Q95 - 2Q96 the projected global increase will likely be over 5000 megawatts. With a typical 90 percent load factor this increase in fab capacity will result in increased electricity sales of some 40,000 gigawatt hours per year. The construction schedule for these plants has tended to slip, however, due to weak semiconductor market conditions in 1996. Updated schedule information is not yet available.

Table 2. Projected Construction Investment and Electric Load Growth for Fabs Announced 1Q95 - 2Q96, U.S. and Rest of World.

	Investment Value ($B)		Annual MW Load Growth		Cumulative MW Load Growth		Annual GWH	
	U.S.	RoW	U.S.	RoW	U.S.	RoW	U.S.	RoW
1994					947	2153	7469	16975
1995	1	8	1	245	949	2398	7478	18906
1996	7	20	199	611	1147	3009	9044	23726
1997	28	48	838	1437	1985	4447	15652	35058
1998	17	26	527	782	2512	5228	19807	41220
1999	2	6	75	185	2587	5413	20398	42674
2000	1	4	28	132	2615	5545	20619	43716
Total	$56	$113	1668	3392				
U.S. plus RoW		$169 Billion		5,060 MW				

Even though we are using relatively crude calculations of electric demand, and the actual construction schedules tend to slip, the projected growth of the industry assures that loads will increase dramatically.

BARRIERS TO INDUSTRY INTEREST IN ENERGY EFFICIENCY

In the past, energy efficiency has not been a high priority area for management concern since energy costs were typically about one or two percent of total production costs, including capitalized land, buildings and equipment. This, combined with the industry's schedule-driven, risk averse and fragmented facility design process has led to plants and production tools which present significant energy efficiency opportunities.

The semiconductor industry faces extreme time pressures to get new products to market. New billion dollar plus fabs are designed and built in 12 - 18 months. Design time is squeezed and the design process is fragmented, precluding whole systems design integration. As an example of how a fragmented design process affects a construction project, consider the effect on the mechanical and electrical designs produced by separate teams each with its own capital budget and under intense pressure to complete work on time. Designers in this situation report there are few opportunities for iterations between the two groups to optimize project capital

costs. Such a fragmented design team is unable to capture for the client the potential capital cost savings in electrical systems which could accrue from a more efficient mechanical system[13].

The risks of design changes are often perceived to be unacceptable. In many companies a bias exists to "copy exactly" the previous plant, thus assuring acquisition of a design that is known to be profitable, and minimizing the perceived risk of design changes. Reliability is a major driver. Conservative, proven design approaches are relied upon to assure owners that their investments will work as well as a previous plant.

Other barriers to energy efficient design include obsolete standard design rules-of-thumb based on out-of-date technologies, architect's design aesthetics versus the needs for good mechanical design layout, lack of awareness of high efficiency design and the benefits that it may create, and lack of benchmarking for energy costs[14].

CHANGING INDUSTRY ATTITUDES TO ENERGY EFFICIENCY

It is our observation that industry is beginning to take a greater interest in energy efficiency. Our interviews suggest several reasons for this change, including economics, increasing process energy intensity, increasing pressure to improve productivity, increasing expectations that international standards might affect the price and or availability of energy resources, and increasing emphasis on corporate environmental performance.

Economics

Electricity costs in new factories are often the single largest operating cost, exceeding even salaries and benefits (operating costs exclude capitalized land, buildings and equipment). Electricity bills of $1 - $2 million per month are common. Considering the industry plans to invest $169 billion in new plants, they are committing almost another $30 billion in present value electricity costs or almost 18 percent of total capital investment. As competition in the industry tightens margins, these numbers are becoming obvious targets for management attention. Equally important, the industry shares a common concern about raising the capital investment required for new plants to manufacture the next generations of technology. Trimming operating costs could provide several billion dollars to help fund next generation plants.

Increasing process energy intensity

Two trends, smaller feature sizes and increased chip complexity, are driving increases in process energy intensity. Smaller feature sizes require cleaner and cleaner manufacturing environments, increasing the energy used for air movement and filtering. Increased complexity requires more layers on each chip, hence more process steps and more direct manufacturing energy per chip.

Productivity

The industry is looking for new ways to improve productivity. The 1994 National Technology Roadmap notes that the historical methods of making productivity gains are no longer as effective and that the industry needs new approaches if it is to continue reducing costs at a 30 percent per-year per-function clip.[15]

International standards may affect energy price or use

Negotiations to implement the United Nations Framework Convention on Climate Change initiated at the Earth Summit in Rio could have an effect on industrial energy use and prices. The Framework Convention was ratified by more than 100 nations including the U.S. It requires that ratifiers stabilize atmospheric concentrations of greenhouse gasses, but with no specific target levels or timetables. The Berlin Mandate, adopted in 1995 at a conference of the parties to the Framework Convention, requires countries to negotiate binding protocols by 1997 and negotiations are currently underway.

The United Nations Environment Program Insurance Industry Initiative, with signatories including 62 major global property casualty insurance and reinsurance companies from Europe, Africa, Asia, North America and Australia wrote that "Human activity is already affecting climate on a global scale. ... In the case of climate change risks, the most efficient precautionary measure is a substantial reduction of greenhouse gas emissions with respect to a 'business as usual' scenario of greenhouse gas emissions."[16]

Climate change policy impacts are already being felt by the semiconductor industry as it works to reduce emissions of perfluoro compounds ("PFC") which are highly potent global warming agents. Regulation of carbon dioxide emissions from energy use is a relatively short step from the industry's PFC experience.

The effects of climate change policy on energy prices or regulation may vary in different areas of the world, perhaps affecting the relative economics of a firm's plants. For those companies active in several areas of the world the presence of a more stringent standard in one area may influence adoption of that standard by the firm in all it's global locations. This has already occurred in other industries and other contexts.[17]

Corporate environmental performance

Some firms recognize the strategic benefits of energy efficiency as part of their corporate positioning on environmental issues. According to Fabio Borri, the Director of Corporate Environment Strategy for SGS-THOMSON Microelectronics, "We consider that environmental performance is a basic ingredient for product quality and company reputation; the business benefit is that managing for natural resource efficiency and clean processes is one of the greatest engines of productivity improvement."[18]

INDUSTRY INITIATIVES TO INCREASE PRIORITY ON ENERGY EFFICIENCY

Responding to these issues, several initiatives are focusing the industry's attention on energy efficiency. Among these are the following.

* The industry research consortium SEMATECH, through its Environment Safety and Health program, initiated in late 1996 an international facility energy audit and benchmarking program.

* SGS-THOMSON Microelectronics has adopted an environmental management and audit scheme with the intention of becoming the greenest chip producer in the world.

* Some semiconductor manufacturers, notably Cypress Semiconductor and Hewlett Packard, have become Climate Wise Partners.

* Several firms in the facility design and construction field are investigating energy efficient design.

* Several semiconductor manufacturers have initiated senior management reviews of the role of energy efficiency and set energy use reduction goals on the order of 4 to 5 percent per year.

* A design/build contractor and its client (Supersymmetry Services and Western Digital) won the Association of Energy Engineers "1996 Energy Project of the Year" award for implementing a state of the art energy efficient clean room design in a factory in Kuala Lumpur.

* In Portland, Oregon two firms (LSI Logic and Fujitsu) have agreed as a condition of property tax incentives to implement "exemplary" environmental management plans that include energy, water and resource efficiency components.

* In the transition from 200 to 300 millimeter diameter wafer processing the industry has defined design protocols to improve resource efficiency of the next generation of manufacturing tools.

EXAMPLE OPPORTUNITIES TO IMPROVE ENERGY EFFICIENCY

Several examples are presented below to illustrate technical opportunities. The first involves improvements to the furnaces used to produce single crystal silicon ingots, from which silicon wafers are produced for use by the semiconductor and photovoltaic industries. The second involves design of high efficiency HVAC systems for clean rooms. Several additional examples in semiconductor fabs are briefly summarized.

Efficiency opportunities in silicon crystal growing furnaces

About half of all U.S. semiconductor-grade crystal and wafer production is located in the Pacific Northwest. The electric resistance-heated "Czochralski" ("Cz") furnaces in these facilities produce, or "grow," single-crystal silicon ingots. From these ingots thin wafers (700 micron) are made for the semiconductor industry. The photovoltaic industry uses even thinner wafers, now about 350 micron and moving to 200 micron.[19]

For semiconductor-grade ingots and wafers the furnaces typically are operated in a clean room environment, due to purity requirements. Photovoltaic-grade ingots do not require such purity and are operated in a more conventional industrial building.

The semiconductor industry dominant ingot and wafer diameter is now 200 mm (8 inch). The industry is now in transition to 300 mm (12 inch) wafers, with equipment to process these planned to be available in 12 - 18 months. In the photovoltaic industry 150 mm (6 inch) is the dominant diameter.

Depending on the diameter of the ingot to be produced, a furnace may have a nameplate rating of 125 - 250 kW or more. The duty cycle is 24 hours, with power on for 18 hours to melt the silicon and grow the crystal, and power off for 6 hours to accommodate maintenance and reloading. Furnaces we have observed normally operate at about 2/3 rated power. A factory with 100 furnaces with nominal 250 kW rating would produce furnace-only electric loads of 16.5 megawatts and about 104,000 megawatt hours per year.

Siemens Solar Industries, the largest photovoltaic manufacturer in the world, grows silicon ingots in their Vancouver, Washington plant. Growing rapidly, Siemens expects to treble its crystal growing capacity every few years. The PV industry, presently manufacturing about 90 megawatts per year, hopes to ramp up to between 1000 and 5000 MW/Yr. Crystal growing is the rate limiting factor in photovoltaic production and as such has attracted management attention to increase productivity.

Siemens' executives have described several improvements to crystal furnaces that are in their R&D plans. Design improvements to the furnace hot zone and argon gas management system, and improved heat transfer from the crystal as it is grown, can be combined, they estimate, to yield impressive results, including 60 - 75 percent reduced energy use, 90 percent reduction in expensive argon gas, and most importantly, perhaps a 33 - 50 percent shorter cycle time for crystal growth.

They write, "For the case of 15% efficient 350 micron thick cells ... efficient conventional Cz crystal growing operations would require between 75 and 100 growers to produce 100 MW/yr, depending on the percentage of full term ingots grown. ... With the use of improved hot zones, which allow faster pull rates, the number of growers required to produce 100 MW/yr decreases to about 50."[20]

Siemens' executives believe these improvements would be applicable to the entire installed base of Cz furnaces used to manufacture ingots for the semiconductor industry. If achieved, this would reduce industry capital requirements, reduce costs for both semiconductor and photovoltaic grade wafers, significantly reduce energy use required for industry growth, and increase the economic viability of photovoltaic power systems.

In the economics of this case, the value of such a huge increase in furnace productivity completely overwhelms the value of the energy savings. One can imagine a fairly rapid technology diffusion if this package of retrofits is proven. Wafer manufacturers will have to adopt this technology for productivity reasons to remain competitive.

Semiconductor fab clean room HVAC systems

HVAC systems represent about 30 percent of the electric load of a typical semiconductor fab. In the industry's conventional design practice, HVAC system performance, including chillers, pumps, fans and cooling towers, can range from 1.2 - 2.0 kW/ton of chiller capacity.

In 1995 and 1996 workshops sponsored by the Northwest Power Planning Council, Lee Eng Lock of Supersymmetry Services (Singapore) presented data on clean room HVAC design performance at 0.6 - 0.7 kW/ton. He concluded that 70 percent or greater energy efficiency improvements over industry standard practice in fab HVAC systems are achievable at a lower net capital cost than conventional practice.

Benefits of an integrated, high efficiency design approach in new facilities go well beyond reduced capital cost and energy cost savings. Lee reported that facility reliability can be enhanced by reducing wear and tear on components such as filters, fans, pumps and motors.

Examples of component efficiencies for both conventional and high efficiency design practice are presented in the following table.[21]

Table 3. Clean Room HVAC Design Budget -- kW per Ton per Component.

System Component	Typical Design	Efficient Design
Chiller	0.6	0.5
Air Handler	0.6	0.06
Chilled Water and Condenser Water Pumping	0.3	0.04
Cooling Tower	0.1	0.01
Total kW/Ton	1.6	0.61

Of potentially great significance to the industry, though as yet poorly documented, is that highly efficient HVAC systems based on Lee's design strategy may improve performance of filter and frame assemblies, and provide better contamination control. Low Face Velocity ("LFV") coil designs, developed at the University of Adelaide, Australia, are employed in these designs.[22] LFV uses about double the area of a standard coil, and cuts the coil depth in half, permitting face velocities to drop from 400 - 500 feet per minute to the range of 150 - 225 fpm. This greatly reduces system pressures, putting less stress on filters and frames.

Discussions with fab facility managers indicate that many have experience with filter frames that have gradually become bent from the high pressures used in conventional face velocities, resulting in particles leaking around the filters. To our knowledge, the effect of the low face velocity design strategy on long term filter performance, contamination control and production yield has yet to be researched and documented. We believe this is an important area for additional research.

Adequate monitoring and analysis of clean room HVAC system performance is a central strategy necessary to maintain high efficiency operation. Using precise and reliable metering equipment, which can be relied upon for the life of the plant, coupled with sophisticated data visualization software, can permit effective analysis and use of data acquired at even one minute measurement intervals. Since data storage is cheap and getting cheaper, such data can be permanently archived over the life of the central plant and used to verify system performance and diagnose operating conditions.[23]

As noted above, fab energy audit benchmarking activities are now underway in the semiconductor industry. Metering and data visualization protocols such as these can provide the industry with the capability for real time benchmarking. This could be especially useful for a company with multiple fabs in various areas of the world. An internet or intranet environment could be used to allow easy comparisons.

Additional opportunities

In addition to the HVAC system, a semiconductor fab facility contains production tools and several key support subsystems, including vacuum, exhaust, ultrapure water, process cooling water, compressed air, specialty gas production (e.g. nitrogen, hydrogen), waste treatment, lighting. In our research numerous interviews identified opportunities with very large savings associated with each area. These reported opportunities ranged on the order of 50 to 80 percent energy savings. Some, for example light guides, have beneficial productivity effects that can have significantly greater value than associated energy savings. Examples of reported efficiency improvement opportunities in fab tools and systems include:

Production tools — Estimates of 50 - 70 percent efficiency improvement opportunities were reported in the course of our research. Tool manufacturers have recently begun to consider the value of these potential savings to their customers.

Vacuum — New scroll technology vacuum pumps reportedly reduce electric use 80 percent compared with conventional technology used to produce initial stages of vacuum ("rough-in" vacuum) required for certain tools.

Exhaust — Exhaust levels are reported to be typically six times greater than safety codes. SEMATECH has a technical advisory group investigating exhaust optimization.

Ultrapure water	Pressure drops in advanced membranes used for reverse osmosis process may be able to be reduced, perhaps by 2/3, from 600 psi to 200 psi.
Process cooling water	A separate chilled water plant, and/or free cooling with heat exchangers, can more efficiently serve the PCW load, rather than using the HVAC system chillers.
Lighting	Light guides with external sources could allow fabs to avoid the practice of overlighting and subsequent group relamping, while reducing particle contamination shed from lamp pin contactors. Group relamping is highly intrusive in a fab clean room environment, requiring expensive interruption of production. Remote light sources can be highly efficient, such as sulphur, other HID lamps, or concentrated daylight.

STRATEGIES TO MOVE THE MARKET

The barriers that have slowed implementation of efficiency improvements in the microelectronics industry are substantial. The activities and strategies described below can help to counteract the barriers, improve industry resource efficiency, and help the industry to prosper in several key ways:

* Save money: Capital and operating costs would be reduced.
* Improve performance: Environmental controls and productivity would be improved, while providing continued assurance of reliability.
* Reduce environmental impacts: Emissions at the facility, as well as at the electric utility would be reduced, hence reducing industry exposure to emerging international concerns regarding climate change.
* Improve corporate citizenship: An additional result would be better community relations because of perceived environmental responsibility and reduced demands on local infrastructure.

The strategies listed below are designed to test new technologies and provide defensible data to support the microelectronics industry in overcoming the barriers to efficiency. They will be most successful if supported by collaborative efforts of people within the microelectronics industry, as well as with others in the energy and energy efficiency industries; with tool and other product manufacturers and vendors; and with local, state and federal government agencies.

Develop case studies

Support the development of case studies, including measured, detailed energy performance data. This data will provide facility owners with objective information with which to evaluate the performance of their facilities and processes. The SEMATECH International Energy Project, which is designed to produce benchmark energy analyses, is one example of this type of activity. Such data could be produced at the level of individual factories and process tools. Key to this strategy will be development of protocols for measuring and visualizing energy performance, and wide distribution of the data, on the internet for example, so it can be readily studied and implemented elsewhere.

Create ongoing education opportunities

Organize continuing professional education, including an information exchange network, where design professionals are provided opportunities to learn from industry innovators. The Northwest Power Planning Council and the Oregon Office of Energy have begun this process in the Northwest by sponsoring annual workshops with Lee Eng Lock of Supersymmetry Services. Other resources could include an internet web site where energy and resource efficiency information could be collected and made available.

Improve energy efficiency in next generation production tools

Integrate design for energy efficiency with industry tool manufacturers. We recommend that a charrette process be used to integrate diverse perspectives into the design process (see charrette description below). The charrette process, which has been used successfully in other industrial efficiency projects, can be used at any

scale, from entire factory systems to individual process tool designs. The new tools to be deployed for the 300-millimeter wafer transition are a potential candidate for this process. Redesigned tools could then be independently evaluated to determine their cost of ownership.

Produce efficient design guidelines

Publish energy-efficiency oriented design guidelines. These could be developed collaboratively by parties with energy-efficiency expertise, organizations representing the microelectronics industry and other interested parties. Lawrence Berkeley National Laboratory and the California Institute for Energy Efficiency recently published a Design Guide for Energy-Efficient Research Laboratories.[24] This guide could serve as a useful platform on which to build a more comprehensive design guide for production clean rooms.

Assess future technology

Track advanced research and development activities that are focused on alternative production regimes for tool systems, including enhanced mini-environments and self-contained cluster tools. Facilitate the integration of energy-efficiency aspects into designs for prototype and conceptual models. The Semiconductor Research Corporation and its university-based research centers, and SEMATECH, with support from energy efficiency design experts, could be venues for these activities.

Provide industry roadmap assistance

Provide objective information from an energy-efficiency and environmental perspective to inform the industry's "National Technology Roadmap for Semiconductors". The Roadmap is the industry source for planning technical research and development activities. It is revised every three years and would provide an effective context to articulate goals related to reducing industry energy use, while improving economic performance and reliability.

Support research and development projects

Support potentially high-impact research and development projects designed to improve energy efficiency in specific technical systems. Funding from organizations concerned with advancing energy efficiency (e.g. emerging electric utility consortia with interests in market transformation), participating industrial firms and industry associations, could be linked with appropriate technology transfer and commercialization commitments. Four examples illustrate this type of activity:

1. Silicon ingot furnaces: As discussed above, Siemens estimates that research and development investments can improve energy efficiency by more than 50 percent, reduce use of expensive argon gas by 90 percent and potentially double furnace productivity. These technical improvements are reported to be applicable to the entire global base of crystal growing furnaces.

2. Lighting: Light guides, an advanced lighting distribution technology, use a remote light source and distributes light through plastic tubes. This is a candidate to replace standard fluorescent lighting in clean rooms, and could save fab owners the expense and contamination problems in relamping clean rooms.

3. Dry cleaning technologies: New microelectronics fabricating plants require on the order of a million gallons of water every day, a significant portion of which is used for cleaning. Dry clean technologies (cryogenic, laser or plasma) are being developed that promise better particle removal efficiencies, yet require far less water and reduce wafer processing time. The tradeoffs between energy and water use in dry clean technologies are worth investigating.

4. Low face velocity coil design: To what extent can LFV design influence clean room contamination control? A research plan to investigate this question should be carefully developed and implemented.

Use design charrettes to build collaboratives and enhance creativity.

Charrette is French for cart. It refers to the historical practice used by French architecture students to cart their semester projects to the design review. Working in teams, these students were intensely involved in the creative process, constantly working with each other to refine their designs. This process was at its most

intense as the teams were carting their designs to their professors. Hence, the term charrette has come to mean a short, intensive, team-work oriented design process.

Today, charrettes are intensive workshops that bring together a multidisciplinary team in a creative design process that may span several days. This team performs a detailed, systems-oriented analysis of existing and proposed designs, and recommends design changes and improvements. Follow up after the charrette phase is critical; generating ideas is only the first stage. It is also important to evaluate cost savings, reliability and economics; select the best package of options; work with designers to integrate the best options into the design; and complete the feedback process with user and post-occupancy evaluations.

Participants would span such disciplines as energy efficiency design; maintenance; manufacturing; facilities design; marketing; finance; environment, safety and health. If focused on a fab, the team should include the company's architect and consulting engineering firm, including mechanical, electrical and structural specialties, as well as specialists in resource-efficient design. The charrette team would analyze all energy using systems in the plant and see where efficiencies can be realized.

Design charrettes to address green fabs and green tools could be effective in breaking through many of the technical and market barriers to improved energy efficiency in this industry. Examples where such a process could be effectively employed in the microelectronics industry include:

* A company with a fab that has been planned, but delayed due to market conditions,
* A company with a phased-construction plan for multiple fabs over a long time period,
* A company that wants to make environmental management a part of its corporate citizenship and market positioning,
* An engineering firm with an interest in improving the efficiency of its standard fab design,
* Process tool manufacturers planning the next generation of tools, as in the 300-millimeter wafer transition,
* Companies wanting to make improvements to mechanical and electrical systems in existing facilities.

For design charrettes to be successful, participants will need to:

* Provide the right mix of staff, consultants and process facilitators,
* Allow time to innovate outside of production schedule time pressures, and
* Follow through, measure results and incorporate findings in the next plant or tool design.

As semiconductor manufacturers acquire experience with more efficient designs and processes, there is a high probability that the new approaches will become standard practice. After each engineering firm has thought through the design issues, developed an effective green fab plant design, and built and evaluated it for a customer, it is likely that these engineering companies will use this experience in their marketing and business positioning. In short, the design market will be transformed to a new level of resource efficiency. Similar results are expected in the production tool market.

CONCLUSION

Growth in the semiconductor industry is occurring on an exponential scale that will soon place it among the top employers worldwide. Over the next few years, approximately $169 billion is planned to be invested in new microchip facilities. If current trends continue, this growth will place significant demands on electricity and water resources in the communities into which it expands.

Preliminary investigations of efficiency opportunities in the industry indicate that significant energy efficiency improvements are possible through adoption of best practices and integrated design strategies. Unfortunately, the pressures on the industry to grow and meet enormous technological challenges have created substantial barriers to adoption of these efficiency opportunities. A variety of creative strategies may be implemented to overcome these barriers. These strategies include some traditional efforts such as design assistance, education on best practices, case study development, and benchmarking.

Large benefits will be derived from new ways to get cross-discipline design integration and the involvement of non-industry efficiency experts that can bring fresh ideas and best practices to the design process. One application of this approach would be to initiate a collaborative design charette process for microelectronics fabrication facilities and production tools. If successful, the charette process could provide a mechanism to fully integrate the best of the industry practices, producing deep improvements in energy efficiency, as well as reduced capital cost and enhanced productivity.

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